Adrias: Interference-Aware Memory Orchestration for Disaggregated Cloud Infrastructures

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***Abstract*—Workload co-location has become the de-facto approach for hosting applications in Cloud environments, leading, however, to interference and fragmentation in shared resources of the system. To this end, hardware disaggregation is introduced as a novel paradigm, that allows fine-grained tailoring of cloud resources to the characteristics of the deployed applications. Towards the realization of hardware disaggregated clouds, novel orchestration frameworks must provide additional knobs to manage the increased scheduling complexity.**

We present Adrias, a memory orchestration framework for disaggregated cloud systems. Adrias exploits information from low-level performance events and applies deep learning techniques to effectively predict the system state and performance of arriving workloads on memory disaggregated systems, thus, driving cognitive scheduling between local and remote memory allocation modes. We evaluate Adrias on a state-of-art disaggregated testbed and show that it achieves 0.99 and 0.942 R^2 score for system state and application's performance prediction on average respectively. Moreover, Adrias manages to effectively utilize disaggregated memory, by offloading almost 1/3 of deployed applications with less than 15% performance overhead compared to a conventional local memory scheduling, while clearly outperforms naive scheduling approaches (random and round-robin), by providing up to $\times 2$ better performance.

***Index Terms*—Memory disaggregation, Data placement, Deep Learning, Cloud Infrastructures, Orchestration, Interference**

I. Introduction

Cloud computing has been established as the new standard for application deployment due to the flexibility and cost effectiveness it offers [60]. Cloud systems typically suffer from high resource under-utilization, due to the strict performance requirements of deployed applications, which push providers to dedicate machines for guaranteeing performance [34], [74], [82]. To tackle this under-utilization problem, multi-tenancy [18], [19] has been adopted as the de-facto deployment model for Cloud applications. However, multi-tenancy leads to interference in shared resources, which in turn induces variability and degradation in the performance of applications [25], [26], [59], [65]. As a result, intelligent orchestration and allocation of computing resources is required [25], [44], [58], [85], where complex cluster-wide software mechanisms control how hardware resources are assigned to applications.

Cloud systems typically involve two layers of resource management which are orthogonal to each other and can be applied independently, i.e., *L1)* The initial static allocation of resources and placement of incoming applications (so called resource orchestration) and *L2)* the dynamic adjustment of allocated resources to meet requirements of applications (so called runtime management). Mechanisms in the first category should be able to identify the resource requirements of incoming (possibly unknown) applications, and avoid placements that lead to resource interference, while also considering the underlying HW heterogeneity [9], [25]–[27], [61]. The second layer includes runtime mechanisms that dynamically optimize the performance of running applications, such as SW controllers [19], [29] and/or OS-integrated extensions [87], [91] that regulate resources of deployed applications.

Despite their sophistication, software only mechanisms have been proven incapable of fully resolving the resources under-utilization problem, that is mostly a bi-product of the diverse computational requirements of cloud workloads combined with the fixed resource proportionality of cloud-server systems. As a consequence, it is common in modern data-centers to observe a fragmentation of resources that are available yet not consumable by any workload [42], [46].

To overcome this resource wall challenge, *hardware disaggregation* has been proposed as a new design paradigm [4], [45], [75], [76]. In a disaggregated cloud, the underlying HW infrastructure is organized as pools of heterogeneous resources that can be composed on-demand into compute units tailored around workload-specific requirements. Recent scientific research has examined the applicability of the disaggregated concept to several components of modern Cloud and HPC infrastructures, including processing units [10], [21], [33], [73], memory [32], [57], [72], [84] and storage [10], [48], [53], [66]. In addition, rack-scale operating systems [81] and runtimes [14] have been proposed for dynamically managing disaggregated resources.

Need for memory orchestration: This paper focuses on memory-disaggregated infrastructures addressing the newly induced problem of interference-aware memory orchestration.

In a memory disaggregated system, orchestrated placement to memory resources is required to minimize the impact on applications performance due to the increased latency in accessing remote memory [50]. While prior research efforts have thoroughly examined dynamic runtime mechanisms (L2 – e.g., page migration/prefetching) for memory-disaggregated and multi-tiered memory systems [47], [62], [91], limited work has been conducted with respect to the problem of interference-aware memory placement in disaggregated clouds (L1), since existing scheduling approaches [25], [26], [41] neither target memory orchestration nor been have extensively examined for such composable systems. However, orchestration of memory resources in disaggregated environments is critical for two main reasons: *i)* In presence of interference, determining an efficient memory mapping can significantly improve the overall performance of the application and *ii)* Optimal initial allocation of memory can minimize the amount of data travelling back and forth through the network, e.g., in applications that present a low ratio of hot versus cold pages

Paper Contributions: We introduce *Adrias*[1], an interference-aware memory orchestration framework that enables effective/optimized data placement decisions on memory-disaggregated cloud infrastructures. The key features of Adrias could be summarized through: *i)* its ability to forecast the tendency of system-wide metrics in the future, thus driving proactive memory orchestration decisions; *ii)* its accurate performance predictions for deployed applications w.r.t. memory heterogeneity (local/fast vs. remote/slow DRAM) and interference and *iii)* its power to leverage disaggregated memory with minimal impact on the performance of deployed applications without the employment of dynamic memory management mechanisms. Adrias exploits system-level performance monitoring information and leverages deep learning approaches to place incoming applications on the pool of available memory resources. To the best of our knowledge, this is the first work tackling the problem of interference-aware memory orchestration, i.e. applications' data placement on memory-disaggregated cloud systems. Our main contributions are:

- We perform an in-depth exploration and provide new insights on the performance capabilities of the state-of-art ThymesisFlow disaggregated memory testbed [72]. We characterize ThymesisFlow under various interference scenarios for a set of in-memory cloud workloads, namely Redis, Memcached and several Spark analytics and analyze the impact of memory disaggregation w.r.t. their performance.
- We propose two deep learning models tailored to disaggregated memory systems; *i)* a system state prediction model that forecasts the tendency of monitored performance events in the future and *ii)* a performance prediction model that estimates the performance of applications, when deployed on memory disaggregated systems. Using these models, we are able to accurately predict the tendency of system metrics and performance of incoming applications, achieving up to 0.999 and 0.942 R^2 scores respectively.
- We present Adrias, an orchestration framework for memory disaggregated systems. By leveraging the developed prediction models and a simple, yet effective, scheduling logic, Adrias employs remote memory efficiently, by offloading up to 35% of best-effort applications with less than 15% performance degradation compared to a local DRAM memory allocation approach and also provides comparable QoS guarantees for latency-critical ones.

[1]Adrias was a WWII battleship that hit an underwater mine and was split in two parts but managed to survive and return to service.

II. Related Work

Memory Disaggregation: Memory disaggregation is not a new subject of study, with several approaches appearing over the years. There are fully software-based approaches that expose remote memory as Linux swap devices or rely on RDMA transfers to be explicitly programmed for moving memory blocks to/from remote memory [3], [32], [52], [68], [77], [81], [86]. Efficient use of RDMAs often involves having to reserve and pin chunks of memory beforehand, leading to inefficient utilization of memory resources. A number of full hardware solutions have also been proposed [14], [35], [72] that although different, they are all mostly based on intercepting low level CPU memory operations to process and forward them towards remote systems.

▸ In this work we focus on the ThymesisFlow open-source hardware [72] that requires zero modifications to existing applications and it integrates seamlessly with the Linux memory management system.

Cloud Resource Orchestration: Prior research works have proposed solutions both for static resource allocation of applications arriving on a cluster [25], [26], [31], [41], [44], [89], as well as dynamic regulation of allocated resources of workloads throughout execution [19], [43], [51], [67], [71], [80], [96]. Moreover, production ready resource orchestrators have also been presented [11], [23], [40], [83], [85], showcasing the need for efficient supervision of resources due to interference in shared resources. However, these works focus on typical cloud infrastructures, that consist of conventional servers. Other scientific approaches examine the problems of application orchestration on disaggregated memory systems [54], [69] and performance modeling [93], however they either rely on emulated prototypes [93] or totally neglect the implications of resource interference in shared resources [54], [69].

▸ Adrias goes a step further, by providing an interference-aware orchestrator for memory disaggregated systems, deployed and evaluated over a real, state-of-the-art testbed.

Memory Management of Tiered Systems: Lately, management of multi-tiered systems and/or disaggregated, heterogeneous resources inside data-center facilities is attracting more attention. Recent research efforts focus on mechanisms that provide dynamic disaggregated memory allocations for VMs [15], [16], [64], efficient prefetchers and replacement policies [47], [55], [56], [62], [63], [91] and cost/performance tradeoffs between heterogeneous memory pools [87].

▸ These works belong to runtime management techniques (L2), are orthogonal to Adrias, since they operate on different levels of optimization and can be utilized complementary.

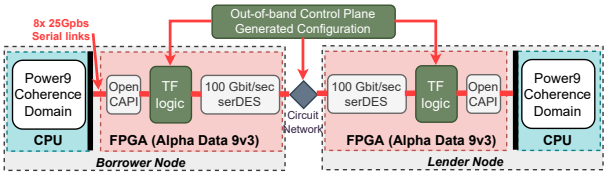


Fig. 1: ThymesisFlow [72] architecture overview

III. Disaggregated Memory Testbed

Prototype Setup: We replicate the ThymesisFlow [2], [72] memory-disaggregated prototype consisting of two AC922 IBM® POWER9™ servers, featuring two sockets with 64 logical cores, 10MB L3 cache per socket and 1.2TB DRAM @2666MHz. Both servers run RHEL (kernel `v5.8.0`) and are equipped with an Alpha Data 9V3 card, that features a Xilinx Ultrascale FPGA. The FPGAs are connected back-to-back using a single copper cable that models a 100Gbps point-to-point connection in a circuit switched network fabric.

Hardware Architecture: Fig. 1 depicts the hardware infrastructure of the ThymesisFlow prototype. On both servers the FPGAs are interfaced to the CPU bus using the OpenCAPI [22] prototcol, that enables coherent access to the CPU memory from an accelerator. The interface between CPU and FPGA is based on 8x25Gbps serial links for a total of 200Gbps. On the borrowing side, the OpenCAPI accelerator is mapped at a specific physical location in the CPU bus that can be then hot-plugged as regular memory. On the lender side the OpenCAPI accelerator accesses the memory on behalf of the borrower by totally bypassing the lender CPU, thus avoiding any unnecessary overhead. ThymesisFlow enables byte-addressable disaggregated memory that does not require any software support such as in the case of solutions based on RDMA [32], [62] and those enabling disaggregated memory by means of a Linux swap device [3], [86]. Every time a memory access performed at the borrower side causes a last level cache miss or flush, the cache line is refilled/flushed via remote memory. An OpenCAPI transaction (read or write) is generated by the borrowing CPU and received by the FPGA. Here the transaction address is modified to a valid one at the lender side and the operation traverses the circuit network (100Gbps) towards the FPGA at the remote node, where the OpenCAPI transaction is re-issued on the bus towards the memory. Responses in case of a read follow the reverse path.

Software Architecture: From the software standpoint, the two servers in the prototype are not symmetric. ThymesisFlow enables the borrower-lender model, where the lender gives away part of its local memory for access from a remote borrower. On the borrower server, ThymesisFlow exposes disaggregated memory as a CPU-less NUMA node, that can be attached using the `libthymesisflow` library. This allows users to avail of all Linux default NUMA-aware functionalities. Alternatively, users can either hotplug the disaggregated memory to the running Linux system in the borrower server, or keep it out from the Linux kernel memory management system and use custom memory allocators. In this paper, we hotplug the disaggregated memory and we control how applications access it by means of ad-hoc Linux cgroups.

IV. Characterizing Memory Disaggregation

We analyze the impact of resource contention on the ThymesisFlow memory disaggregation testbed. We unveil important insights concerning both potential hardware limits of memory disaggregated systems and the impact of interference on the performance of applications leveraging remote memory.

A. Examined Workloads

Cloud infrastructures typically host two types of workloads, best-effort (BE) and latency-critical (LC) ones. The former require the highest possible throughput while the latter have strict QoS guarantees. To cover both types of applications, we examine the following open-source, in-memory applications:

- **Redis (LC):** Redis [17] is a NoSQL key/value store that keeps data in memory. We examine the impact of local and remote memory allocation modes on Redis server instances, serving user requests.
- **Memcached (LC):** Memcached [28] is a distributed memory object caching system, used to cache data and objects in the main memory.
- **Spark in-memory analytics (BE):** Apache Spark [94] is an analytics engine for large-scale data processing. We evaluate 17 different spark applications derived from the HiBench benchmark suite [39], using the default Spark parameter configuration and the *small* dataset as described in [39]. We study the impact of disaggregated memory only on the executor processes, which perform all the task computations.

Load generation: We use asymmetric load generation on the underlying system, by co-locating LC, BE and iBench [24] interference microbenchmarks, as described in SectionV-B1. For LC workloads, we utilize the `memtier_benchmark` [1], i.e. the official Redis Labs' utility for load generation of NoSQL key-value databases. Tail latency is measured using a set of closed-loop memtier clients [79] over asymmetric co-located workloads. More in detail, our setup spawns 4 threads, where each thread spawns 200 clients, i.e. eliminating client-bias [49], [97]. We use a SET:GET ratio of 1:10 and generate a constant load of 10000 and 40000 requests per client. This configuration leads to a total of approximately 30.000 and 100.000 operations served per second for Redis and Memcached respectively, which closely relate to realistic loads found in production, e.g., Facebook services [5], [90].

B. Limits of HW memory disaggregation on ThymesisFlow

We first assess the capacity of our testbed while performing memory operations, by examining the effect of repeated data movement between the local and remote system. In more detail, we spawn an increasing number (1 to 32) of memory bandwidth interfering micro-benchmarks [24] and force them to use memory borrowed from the remote node, thus generating traffic on the link between the FPGA devices in the ThymesisFlow testbed. To highlight interference effects, we monitor system-level metrics related to the local system and

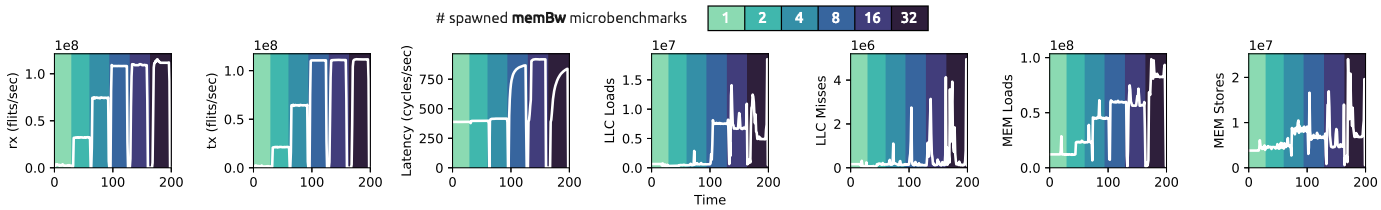


Fig. 2: Capacity of our memory disaggregated testbed for different stressing scenarios. Different color shades denote different number of memory bandwidth stressing microbenchmarks [39] deployed on remote memory mode.

the network interconnection. Specifically, for the local system we gather the Last Level Cache (LLC) loads and misses, and the memory loads and stores, whereas for the FPGAs we measure the number of flits (32B) received (`rx`) and transmitted (`tx`), and the average latency on the ThymesisFlow communication channel. Fig. 2 shows the results and also reveals three important remarks (R1-R3).

R1) Bounded throughput: The throughput of the disaggregated memory reveals an upper bound in the amount of transferred data, with a cap of approximately 2.5Gbps[2]. This value reveals that remote memory has approximately a three orders of magnitude lower bandwidth threshold compared to conventional DDR4 memory systems, which can support a theoretical of 120GBps sustained memory bandwidth [78].

R2) Communication latency: For low to medium amounts of generated traffic (1 up to 4 memory bandwidth microbenchmarks) the average latency on the communication channel follows a steady state of approximately 350 cycles/sec. However, in cases of increased traffic (8 up to 32 microbenchmarks) the latency is almost tripled, reaching a yield plateau of 900 cycles/sec. Until the 4 micro-benchmark, the prototype is capable of handling the memory requests received and the latency remains constant across all executions, while bandwidth increases steadily. From 8 micro-benchmarks onwards, the channel is saturated (bandwidth plateau) and the back-pressure mechanism implemented in the FPGAs starts delaying memory transactions, hence the step in latency.

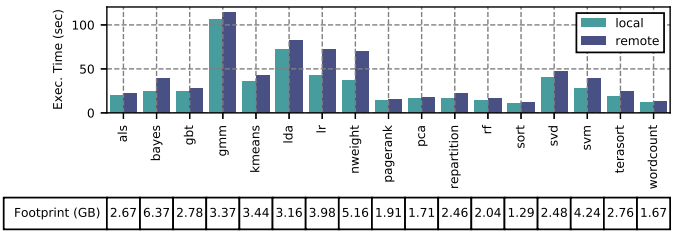
R3) Local system interference: Application deployment on remote memory also induces interference on the memory hierarchy of the local system. This is expected for chip-level metrics (e.g., LLC Loads and Misses), as the cache memory hierarchy lies beneath the abstraction layer of local/remote memory accesses. Regarding memory loads and stores, remote pages are memory-mapped and handled through an enhanced `numactl` memory controller and, thus, all remote traffic is handled on-chip by memory controllers of the local node.

C. Workload characterization

We further quantify the impact of local and remote allocations on the performance of our applications when executed in isolation and under different interference scenarios.

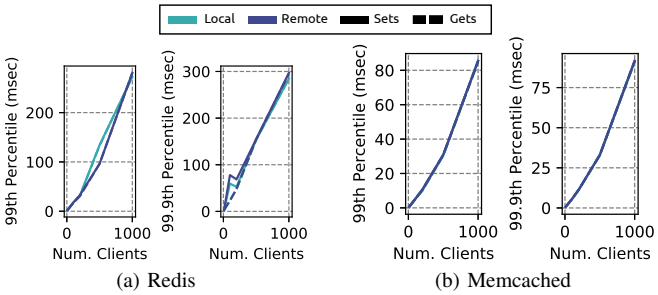
Execution in isolation: For LC applications (Redis, Memcached), we examine the 99*th* and 99.9*th* response percentiles

[2]Given that each flit is 32B, we compute `rx` and `tx` bandwidth in b/s by multiplying with 32*8 [72].



Footprint (GB)	2.67	6.37	2.78	3.37	3.44	3.16	3.98	5.16	1.91	1.71	2.46	2.04	1.29	2.48	4.24	2.76	1.67

Fig. 3: Spark performance characterization (total execution time) when executed in isolation on local and remote memory.



(a) Redis (b) Memcached

Fig. 4: Tail latency of LC applications with increasing RPS when executed in isolation on local and remote memory.

(tail latency) under different loads by scaling the number of clients requesting `Set` and `Get` operations. For BE (Spark) ones, we examine the execution time of applications for the two memory allocation modes. Fig. 3 and Fig. 4 show the results for LC and BE applications respectively.

R4) Non-uniform performance variation: For Redis and Memcached applications we confirm the results reported in prior work [72] that local and remote memory provide almost identical curves in terms of tail latency, for all the configurations examined. This similarity in performance occurs due to the fact that in-memory caches perform many small read and write memory accesses with minimal bandwidth pressure requirements, which can be easily attained based on the specifications of our disaggregated system. For Spark applications, we notice an average degradation of 20% over all our examined benchmarks, which, however, is not uniform across all benchmarks tested. For example in Fig. 3, we observe that `nweight` and `lr` suffer almost a ×2 slowdown when ran on remote memory, whereas others, such as `gmm` and `pca` experience less than 10% performance degradation. This reveals that remote memory is suitable for some applications

while it is not the best options for others.

Execution under interference: Last, we investigate the relative performance impact of resource contention on different levels of the system hierarchy, between local and remote memory. We deploy the same application and measure its performance on local and remote memory under the four interference scenarios namely: `cpu`, `l2`, `l3` and `memBw`. For both modes (local and remote), we spawn a different number (1 up to 16) of resource trashing micro-benchmarks [24], targeting different resources on the system (CPU, L2-cache, Last-Level-Cache and Memory Bandwidth), i.e., if the application is deployed on local memory, so are the ibench microbenchmarks and vice-versa. Fig. 5 shows the respective results, where the density of each cell depicts the performance slowdown of the respective scenario between local and remote memory.

R5) Performance chasm under contention: After a certain threshold (typically 16 for `L3` and > 8 for `memBw` micro-benchmarks), the same amount of interference results in much higher performance degradation on the remote memory, reaching up to ×4 additional slowdown in certain cases. Combined with the results presented in Fig.2, we observe that this threshold corresponds to the saturation point in the communication channel of the FPGAs. This is true both for BE and LC applications, with the latter appearing to be more resistant to interference effects. This shows that remote memory gets saturated much more easily than local DRAM, which also confirms our observation regarding the limitation of remote memory bandwidth made in Section IV-B.

R6) LLC vitality: Contention on the LLC has the greatest negative impact for the majority of BE applications. Interference on the LLC leads to consecutive misses, which in turn are translated to increased memory bandwidth due to read/write accesses from/to the main memory. While both LLC and memory bandwidth end up in generating traffic on the channel, we see that data locality and caching is of paramount importance, as intense LLC contention (16 spawned microbenchmarks) leads to the worst possible performance degradation for the majority of the Spark applications. Moreover, a sustained and increased interference effect on the memory network bus, leads to gradual performance degradation, relative to the extent of the underlying interference. Last, since in-memory databases rely heavily on pointer chasing operations, which introduce poor on-chip spatial locality [20], [38], they appear to be less cache sensitive, revealing higher response times only on memory bandwidth interference scenarios.

R7) Stacking interference effects: For certain benchmarks (e.g., `nweight`, `sort`, `kmeans`), we also notice a performance gap between local and remote memory when imposing interference on lower levels of the system hierarchy (i.e., CPU and L2 cache). We call this a *stacking interference effect*. For such applications, we expect the remote memory allocation mode to be a prohibitive option under realistic scenarios, where different resources are congested simultaneously.

D. Affinity of system & workload metrics

Section IV-B revealed that low-level system metrics can provide insightful information regarding the state of the system. Taking also into account the high performance variability shown in Fig. 5, it is evident that being able to project low-level performance events to higher-level metrics of interest (e.g., application slowdown), would allow us to estimate performance solely through the assessment of lower-level metrics. To investigate whether such a relationship exists, we examine the correlation between low-level system and high-level application metrics prior and during execution when deployed using the remote memory allocation mode. Specifically, we generate several deployment scenarios (similar to the ones described in Section V-B1) by randomly co-locating different ibench workloads with the examined benchmarks, and we keep track of the underlying system metrics during execution.

We evaluate the linear correlation between the average system performance metrics 120 seconds prior to application scheduling (x), as well as during execution ($\tilde{x}$), with the application performance, using the Pearson's correlation coefficient. For Spark applications we consider as performance the total execution time, whereas for Redis and Memcached we study the end-to-end latency, the 99^{th} and the 99.9^{th} percentiles. Fig. 6 shows the respective results and clearly reveals the existence of a correlation between certain metrics and the performance of applications. What is of great interest is that runtime metrics reveal a much higher correlation compared to the historical ones, forming our concluding remark:

R8) Predictive monitoring capability: Proactive runtime assessment of the state of the underlying system is feasible and provides useful insights both regarding the system itself, as well as the performance of deployed applications.

V. Adrias Design

The main goal of Adrias is to efficiently orchestrate applications arriving in a disaggregated system, by deciding between local and remote memory modes. Fig. 7 shows an overview of Adrias' architecture. The *Watcher* component continuously monitors and gathers performance events of the underlying system. The *Predictor* exploits Long Short-Term Memory (LSTM) models for forecasting the future state of the system and performance of deployed applications. Finally, the *Orchestrator* utilizes the predictions to decide the memory allocation policies accordingly.

A. Watcher

The *Watcher* component is responsible for gathering performance events from the underlying hardware infrastructure, providing insights on the data flowing through the memory hierarchy of the system. Focus is given on cache- and memory-related performance counters, as well as metrics that depict the status of the communication channel between the local and the remote memory sub-system. Driven by our analysis in Section IV-B, we monitor the following metrics: Last-level cache misses (LLC_{mis}), Last-level cache loads (LLC_{ld}), Local DRAM memory loads (MEM_{ld}), Local DRAM memory

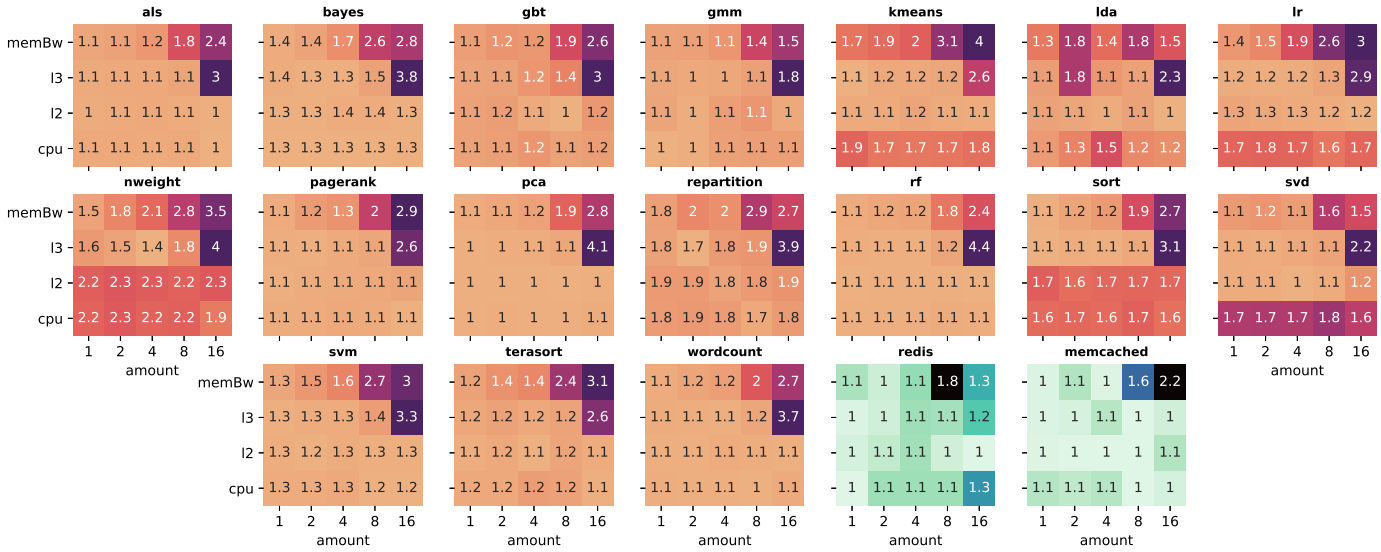


Fig. 5: Benchmark performance characterization under interference on local and remote memory. The heatmap density denotes the execution time and 99^{th} percentile slowdown of remote vs. local execution for BE (orange) and LC (teal) applications respectively, under different interference scenarios (`cpu`, `l2`, `l3`, `memBw`) using iBench [24] contention microbenchmarks.

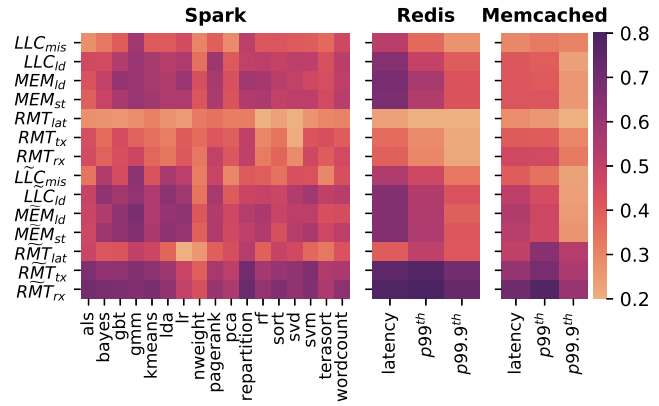


Fig. 6: Correlation of historical (x) and runtime ($\tilde{x}$) system performance events with performance of deployed applications on remote memory.

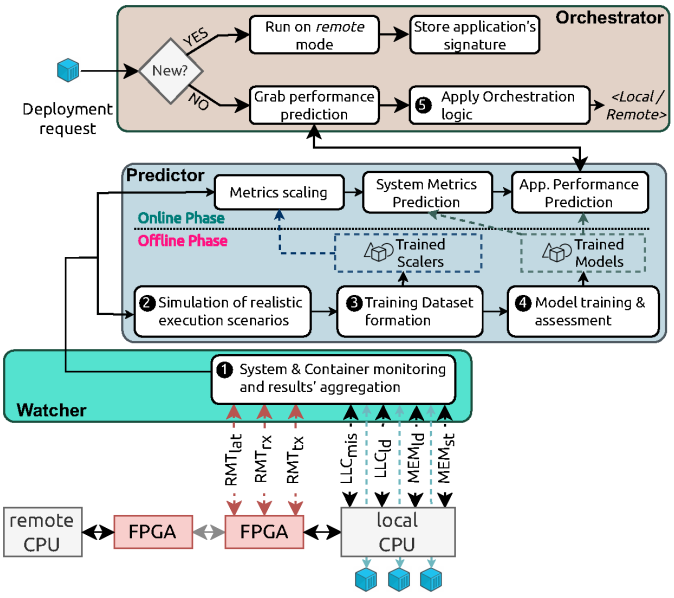


Fig. 7: Overview of Adrias architecture

stores (MEM_{st}), FPGAs communication's channel average latency (RMT_{lat}) and FPGAs receive (RMT_{rx}) and transmit (RMT_{tx}) throughtput. For the CPU performance events of the local system, we utilize Linux's `perf` tool, while the events related to the FPGA channel are directly provided by the ThymesisFlow framework [72]. We set the monitoring interval equal to 1 sec, which, as shown in [30], is a "sweet spot" between inference overhead and QoS violations increment.

B. Stacked-LSTM Predictor

The *Predictor* forecasts the future state of the disaggregated system and predicts the performance of incoming applications w.r.t. the memory allocation mode (local vs remote). The prediction process consists of two phases, *offline* and *online*. The offline phase (design-time) involves three main activities: *1)* collection of representative system metrics' traces that correspond to "realistic" execution scenarios (❷), *2)* generation of the dataset used for training and testing (❸) and *3)* design, train and validation of the prediction models (❹). In the online phase (run-time), the Predictor utilizes the trained models to predict the aforementioned prediction metrics of interest.

1) Offline phase: Interference-Aware trace collection: The first step of the offline phase concerns the collection of interference-aware traces of low-level system metrics (by utilizing the Watcher component of Section V-A). The data collected is used as input dataset for training our deep learning models, described later in this section. This step is vital for the overall functionality of Adrias, since gathering representative

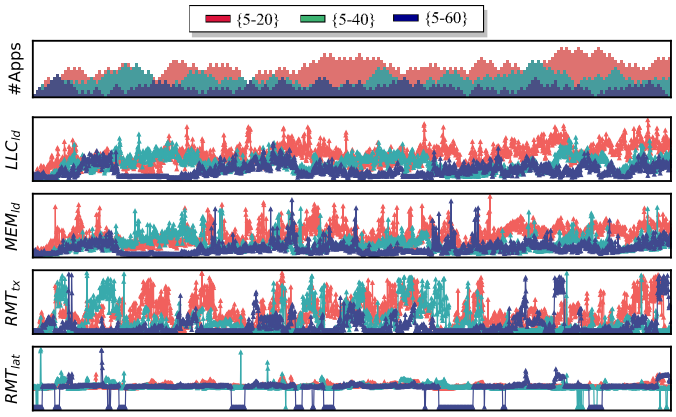


Fig. 8: Number of concurrent applications (top) and performance metrics over time for three representative scenarios. Adrias' data acquisition scheme captures different congestion phases, both within the same and among different scenarios.

data is essential to increase accuracy of any DNN model. **Scenario generation:** We simulate different execution scenarios by employing a random scenario generation approach. Each scenario is characterized by a *spawn interval* $\{t_1, t_2\}$, which denotes the arrival time range of consecutive application deployments on the system. For instance, a spawn interval of $\{5, 40\}$ means that each new application arrives after a random interval between 5 and 40 seconds. Within each interval we pick a random benchmark either from the examined applications, or from the iBench pool and we deploy it randomly on local or remote memory. Through iBench micro-benchmarks, we aim to replicate supplementary interference scenarios that cannot be directly generated by our examined LC and BE workloads. To capture the high dynamicity found in Cloud environments [74], we examine different arrival rates, with sets ranging from $\{5, 20\}$ up to $\{5, 60\}$, where the former imitate more congested scenarios and the latter indicate a more relaxed application arrival pattern. Fig. 8 depicts three exemplary but representative scenarios, assuming heavy ($\{5, 20\}$), moderate ($\{5, 40\}$) and less ($\{5, 60\}$) congested application deployment distributions[3]. As shown, the specific setup exposes a wide variety of phases, both regarding the number of concurrent applications and the spectrum of the monitored metrics.

Insights from scenario execution: Overall, we have simulated 72 diverse 1-hour scenarios with different spawning intervals. Fig. 9 and Fig. 10 show the performance distribution of our examined benchmarks over all the 72 execution scenarios.

▸ Regarding Spark benchmarks (Fig. 9), the use of remote memory has a substantial performance impact compared local DRAM, since the distributions for the scenarios using remote memory expose a tendency towards higher values. However, certain benchmarks (e.g., `gmm`) present overlapping performance distributions, between local and remote memory.

[3]Through the random scenario generation, the maximum number of applications running simultaneously on the disaggregated testbed is 35, with Spark applications spawning 2 worker instances with 4 threads each.

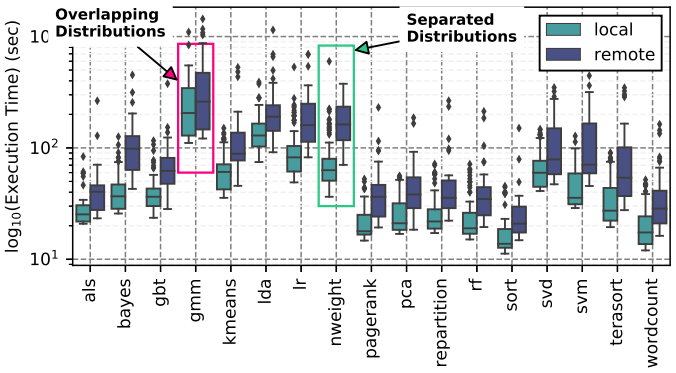
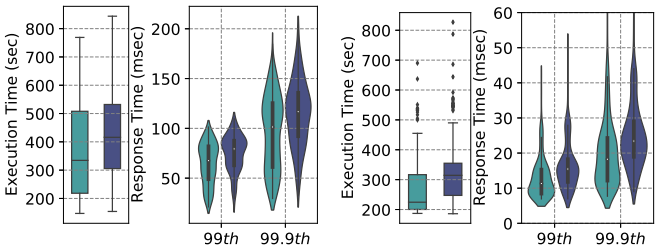


Fig. 9: Spark performance distribution over different execution scenarios.



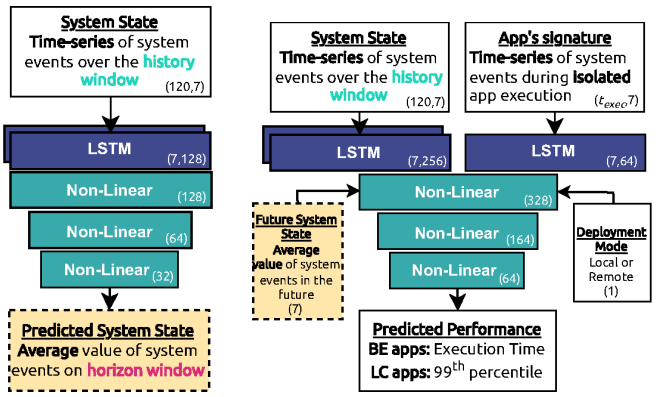
(a) Redis (b) Memcached

Fig. 10: Distribution of total execution time to serve 10.000 requests (left) and of 99*th* and 99.9*th* percentile of response time per request (right) for Redis and Memcached over difference execution scenarios.

This denotes that there might be certain cases where remote memory could provide better performance than local (even if local memory latency is in the order of ~ 80*ns* and remote memory latency ~ 900*ns*), due to high contention in the memory bus of the latter compared to low interference in the communication channel of the former. Moreover, considering that BE applications typically do not have strict performance requirements, we would be able to sacrifice performance to take advantage of the disaggregated memory. In contrast, there are benchmarks (e.g., `nweight`), which, as also described in Sec. IV-C, do not take advantage of remote memory at all, due to stacking interference effects.

▸ For Redis and Memcached, we examine the 99^{th} and 99.9^{th} percentiles, which form typical QoS requirements of LC applications. We observe that remote memory provides higher response times, however we again notice overlapping performance distributions between the two modes. Overall, we anticipate disaggregated memory to be prohibitive for stricter QoS constraints, especially in the Redis case. However, when more relaxed QoS requirements are set, remote memory could be leveraged without violating any constraints.

2) Offline phase - Prediction models training: Adrias utilizes a stacked-model architecture by combining two prediction models one after another: a *system state* prediction model, that forecasts the future values of low-level system



(a) System's state model architecture

(b) Performance prediction model architecture

Fig. 11: DNN architecture of (a) system's state and (b) application's performance prediction models. Parentheses shows the #features and size of each layer.

metrics, and a *performance prediction* model, that receives these predictions (among others) and infers the performance of an application if deployed on local or remote memory. Fig. 11a and Fig. 11b show an abstract view of the models' architecture.

System State Model: The rationale behind this model originates from the observations made in Section IV-D that runtime system metrics are more closely correlated to applications' performance. The model receives as input the *System State – S*, a two-dimensional feature vector containing the time-series values for each examined metric over a history window of length r. We define the system state by considering the metrics monitored by the Watcher component (V-A). As output, the model provides the *Predicted System State* – $\hat{S}$, a vector that corresponds to the predicted mean value of system performance events over a horizon window z. After evaluating different values for r and z , we have determined that a value of 120 seconds provides useful insights both regarding the history and the horizon windows.

Due to the sequential nature of the input, we utilize Long Short-Term Memory (LSTM) [37] layers as the backbone of the model, which has been proven to be extremely accurate in forecasting system level metrics under interference and for deep horizons [30], [65]. The input feature vector is first processed by 2 LSTM layers that identify dependencies between the time-series data and the results are passed to a triplet of non-linear blocks, that combine fully-connected layers with ReLU activation functions, batch normalization and dropout layers to expose non-linearity and avoid overfit.

Performance Prediction Model: This model forecasts the performance of incoming applications, if deployed on local or remote memory. We follow a universal modeling approach, i.e., we build a unique model for all the BE and one for all the LC applications, where the former predicts the execution time and the latter the 99^{th} response time percentile. Although prior research works typically follow a per-application modeling approach [8], [25], [92], we argue that this is not efficient (yet could be more accurate), since building a performance model per application is too time-consuming and requires simulating scenarios for each new application and maintaining a single model per workload imposes serious scalability issues.

Modeling and predicting the performance of applications is a non-trivial task and requires awareness regarding: *i)* the dynamics and sources of interference on the underlying system and *ii)* the inherent characteristics of the application itself and how these characteristics get affected from the current and future status of the system. To uncover this information, the performance models receive as inputs four parameters: The past and predicted system state feature vectors S and $\hat{S}$, the deployment mode (local/remote) and the *application's signature* – k, which is a unique identifier per application, that contains the sequences of monitored metrics during application's execution in isolation on remote memory mode.

The time-series inputs (S,k) are individually processed by two LSTM layers that identify important features in the sequential data. The output results are then concatenated with the deployment mode and the future system state vector $\hat{S}$ to form the hidden representation, which is then processed again by a triplet of non-linear blocks to provide the final performance prediction.

C. Orchestrator

The *Orchestrator* leverages the predicted metrics to proactively assess the state of the system and choose the disaggregated memory policy for deployed applications accordingly. Its design is driven by two fundamentals: *i)* Cloud policies typically apply QoS guarantees for LC workloads and best-effort execution for batch applications [25], [58] and *ii)* Disaggregated memory systems hide dangerous pitfalls (characterization process of Section IV), i.e., disaggregated memory imposes significant performance overhead if utilized recklessly, especially when multiple applications compete over the available resources and, thus, should be leveraged wisely, targeting applications that benefit the most out of it. We tackle the first aspect directly, by introducing a straightforward, yet effective, orchestration logic for BE and LC applications, while the second one is addressed indirectly, through the automatic feature extraction of Adrias' prediction models.

When a new workload is deployed on the system, if Adrias does not own any prior information regarding its *application signature*, it schedules it on the remote memory, captures and stores the respective metrics. Otherwise, it communicates with the Predictor and receives the estimated execution time (for BE) or 99^{th} percentile (for LC) for local and remote memory modes. For BE, we utilize the following discrete function to decide the deployment mode:

$$mode_{BE} = \begin{cases} local, & \text{if } \hat{t}_{local} < \beta * \hat{t}_{remote}. \\ remote, & \text{otherwise.} \end{cases} \quad (1)$$

where $\hat{t}$ is the predicted execution time and β is a slack parameter depicting the maximum performance loss margin that we are willing to sacrifice to leverage remote memory. Choosing β

Event	R^2
LLC_{mis}	0.9969
LLC_{ld}	0.9995
MEM_{ld}	0.9641
MEM_{st}	0.9983
RMT_{lat}	0.9977
RMT_{rx}	0.9871
RMT_{tx}	0.9876
Avg.	0.9932

TABLE I: R^2 score per performance event

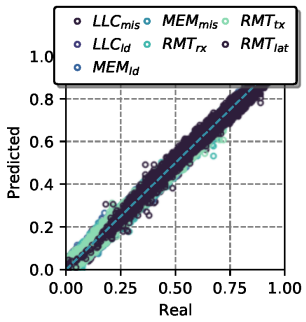


Fig. 12: Performance events predictions' regression residuals

depends on two factors. First, the application itself, as various applications present diverse performance characteristics when deployed on remote memory (Sec. IV). Second, the underlying interference, as overwhelming the remote memory requires greater performance degradation tolerance.

For LC workloads, Adrias aims to utilize remote memory without violating a pre-established QoS constraint. The memory allocation mode is chosen as follows:

$$mode_{LC} = \begin{cases} remote, & \text{if } \hat{p}^{99th}_{remote} \leq QoS. \\ local, & \text{otherwise.} \end{cases} \quad (2)$$

where $\hat{p}^{99th}$ is the predicted 99^{th} response time percentile. Particularly for LC applications, achieving QoS requirements solely through performance assessment during deployment can turn out to be infeasible, due to the unpredictability of the system's future load. In such cases, Adrias can be utilized complementary with other runtime management frameworks, e.g., [19], [67], [91], to dynamically adjust resources.

VI. Evaluation

We implement Adrias[4] using Python (`v3.7.0`), ZeroMQ [36] and the PyTorch library [70]. Adrias imposes minimal overhead on the system, with an average of 300MB RAM utilization and occasional CPU usage spikes of $\approx 15\%$, that correspond to predictions for newly deployed applications.

A. Accuracy Evaluation

We partition the datasets produced during simulation (Section V-B1) in two subsets of 60% (training set) and 40% (test set) of the samples. We examine the accuracy of the system state and performance models for predicting the mean value of monitored metrics over the horizon window and the performance (execution time/tail latency) of applications.

1) System state prediction model: Table I shows the results per metric, by evaluating the coefficient of determination [7] - R^2. Adrias achieves pretty high accuracy, ranging from 0.964 up to 0.999 R^2 score and with an average of 0.993 R^2 overall, illustrating its capability to proactively assess the tendency of system metrics in the future. Fig.12 also presents the actual versus predicted metrics, as there exist cases where a high R^2 score could be counter-intuitive [6]. This plot verifies the strong prediction capabilities regarding the system's state, since the majority of the points lie on the 45^o residual line.

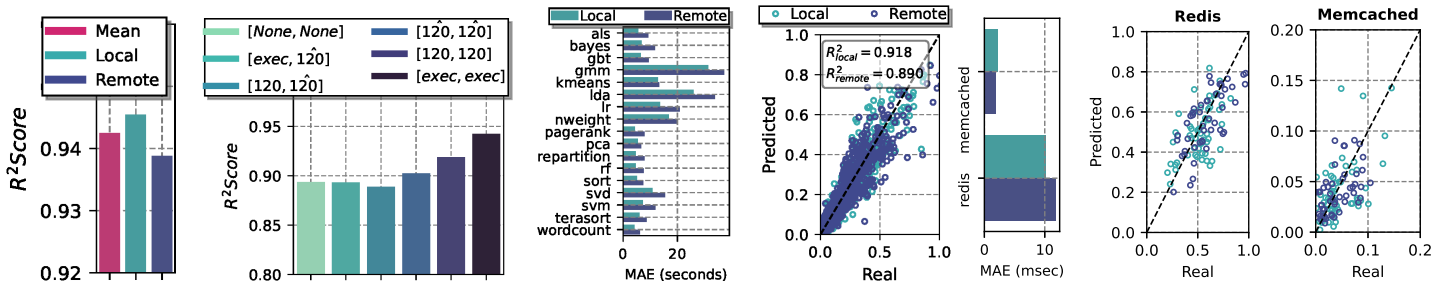
2) Application performance prediction models: As a first step, we train and test the performance models for BE applications, using as the future system state ($\hat{S}$) the actual monitored metrics, gathered during the trace collection process. Fig.13a depicts the respective results, showing that Adrias is able to achieve a $0.942R^2$ score on average, with a slightly higher accuracy for predicting the execution time on local mode ($R^2 = 0.945$) compared to the remote ($R^2 = 0.939$).

Impact of stacked models to overall accuracy: Apparently, the actual future metrics are not available a priori during a realistic inference step. Thus, a reasonable question is: *Should we train the performance models using as "future system state" the actual system metrics, or train using propagated predictions from the system state model?* To answer, we examine the prediction accuracy for different input vectors ($\hat{S}$) during training and testing. Fig.13b shows the results, where the pair $\{x_1,x_2\}$ maps to {train,test} and denotes the type of vector $\hat{S}$ used in each phase. Specifically, *None* implies that $\hat{S}$ was not fed to the model, while $\{120,1\hat{2}0\}$ and $\{exec, e\hat{x}ec\}$ indicate that $\hat{S}$ is calculated from the actual metrics or propagated from the system state model for a window of 120s or for the full duration of the application respectively. The pairs $\{120,120\}$ and $\{exec, exec\}$ give the best accuracy, which, however, are not pragmatic. In practice, feeding the predicted vector $\hat{S}$ to the performance model in the training phase ($\{1\hat{2}0,1\hat{2}0\}$) is the best approach. It is interesting that while the system state model provided very accurate predictions ($0.99R^2$), we still experience an accuracy drop of 3% compared to the theoretical maximum ($\{exec, exec\}$). Moreover, leveraging the predicted future system yields a 2% higher accuracy compared to historical only data ($[None, None]$), thus, verifying the advantage of predictive monitoring.

Runtime accuracy: By employing the $\{1\hat{2}0,1\hat{2}0\}$ approach, we also show the Mean Absolute Error for BE (Fig. 13c) and LC (Fig. 14a) applications and the actual vs. predicted residuals (Figures 13d and 14b). Comparing the MAE with the median performance presented in Fig. 9, the employed DNN models are able to provide accurate performance predictions for both BE and LC applications. Even in cases where we observe high MAEs (e.g., `gmm`, `lda`), these errors correspond to approximately 10% variation compared to the median values of their performance distribution. Overall, we are able to achieve an R^2 score equal to 0.905 for BE and 0.874 for LC.

Generalization on unseen applications: Last, we test Adrias' universal modeling approach ability, by evaluating accuracy using an application-granular leave-one-out validation. Fig.15a shows the R^2 score per benchmark, when excluded during training phase. The model is able to generalize adequately for certain benchmarks (e.g., `gbt`) whereas it fails for others (e.g., `lda`) yielding 0.72 and 0.30 R^2 scores respectively. This suggests that a continuous collection of representative *application signatures* and retraining is crucial for unknown applications. We explore the

[4]https://github.com/pl4tinum/Adrias



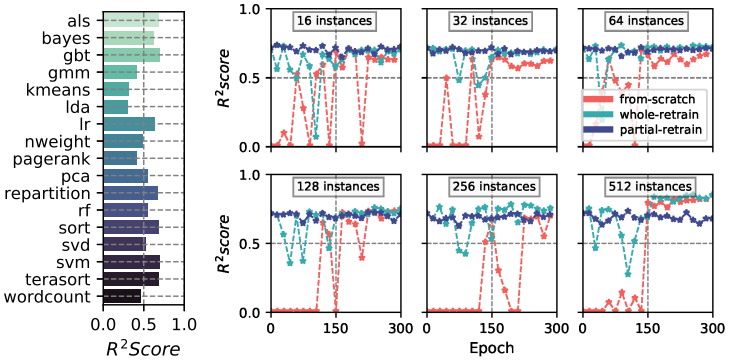
(a) Overall prediction accuracy (b) Impact of real vs. predicted system state on perf. accuracy (c) MAE per Spark benchmark (d) Prediction residuals

Fig. 13: Evaluation of performance prediction model (execution latency) for Best-Effort (BE) applications

(a) MAE (b) Prediction residuals for LC applications

Fig. 14: Evaluation of prediction model (99^{th} percentile) for LC apps

effectiveness of three retraining approaches to improve the accuracy on newly collected data of unseen applications, i.e., *i) from-scratch:* train the whole model from the beginning, *ii) whole-retrain:* retrain all the layers of the model using data from the unseen application and *iii) partial-retrain:* update only the weights of the model that correspond to the application's signature. To avoid bias on the new data during retraining, we set a one-order of magnitude lower learning rate and we feed batches of mixed samples from seen and unseen applications. Fig.15b shows the accuracy achieved and time needed (0.8sec per epoch on a V100 GPU) for different number of training samples for `gbt` application. For lower number of available samples (16-64), whole-retrain results to better accuracy compared to a ground-up training, whereas for higher ones (128-512) it achieves comparable results with less time (epochs) needed. Partial retraining does not improve accuracy over the unseen application, showing the close interrelationship between the application's characteristics (signature) with the dynamics of the system (system state).



(a) Application-granular leave-one-out accuracy (b) Model (re)training accuracy over time (epochs) for various number of samples for `gbt` benchmark

Fig. 15: Performance prediction accuracy for unseen applications (a) and different model retraining approaches (b).

B. Orchestration Evaluation

We compare Adrias with three other scheduling schemes, *i) Random:* mode is chosen randomly, *ii) Round-Robin:* mode chosen in turn between local and remote *iii) All-Local:* all applications allocate local memory.

Adrias' impact on BEs' performance: First, we evaluate the ability of Adrias to utilize the remote memory, without violating the performance threshold introduced through the slack parameter β. Fig.16 (top) shows the execution time distribution of all the examined BE benchmarks and Fig.16 (bottom) the number of times each application got scheduled on the local and remote memory when using the three schedulers and Adrias with different β slack values. For the majority of the workloads, *Random* and *Round-Robin* schedulers provide the worst performance distributions, confirming the need for intelligent orchestration mechanisms. For high betas ($\beta = 1$ and $\beta = 0.9$), Adrias provides identical scheduling decisions with the *All-Local* approach, due to the explicit performance deterioration of the remote memory combined with the implicit accuracy errors of the prediction models. For β equal to 0.8 and 0.7 Adrias achieves to effectively utilize the remote memory, managing to offload approximately 10% and 35% of deployed applications with an average drop of 0.5% and 15% in the median performance over all applications. While the values 0.8 and 0.7 for β would imply an equivalent degradation on the performance of applications, we observe that this is not the case, which is attributed to the accuracy error of the performance prediction model. Finally, for lower slack values (i.e., β=0.6) Adrias offloads the majority of deployed applications to remote memory, which, however, induces significant performance degradation.

Adrias' impact on LCs' performance: Next, we explore Adrias' capability to schedule Redis and Memcached on the remote memory, without violating a pre-established QoS constraint. Based on Fig.10, we define five different QoS levels ($p99^{th}$ response time) of various strictness, i.e., 0 up to 4 per LC application, that correspond to the 87.5^{th}, 75^{th}, 50^{th}, 25^{th}, 12.5^{th} distribution percentiles, where Level 0 denotes the most relaxed and Level 4 the strictest QoS constraint. Fig.17 shows the total number of violations (left) and offloads (right) for all the schedulers. *Random* and *Round-Robin* schedulers provide the worst possible results, since they introduce the highest numbers of QoS violations both for Redis and Memcached, whereas *All-Local* outperforms the

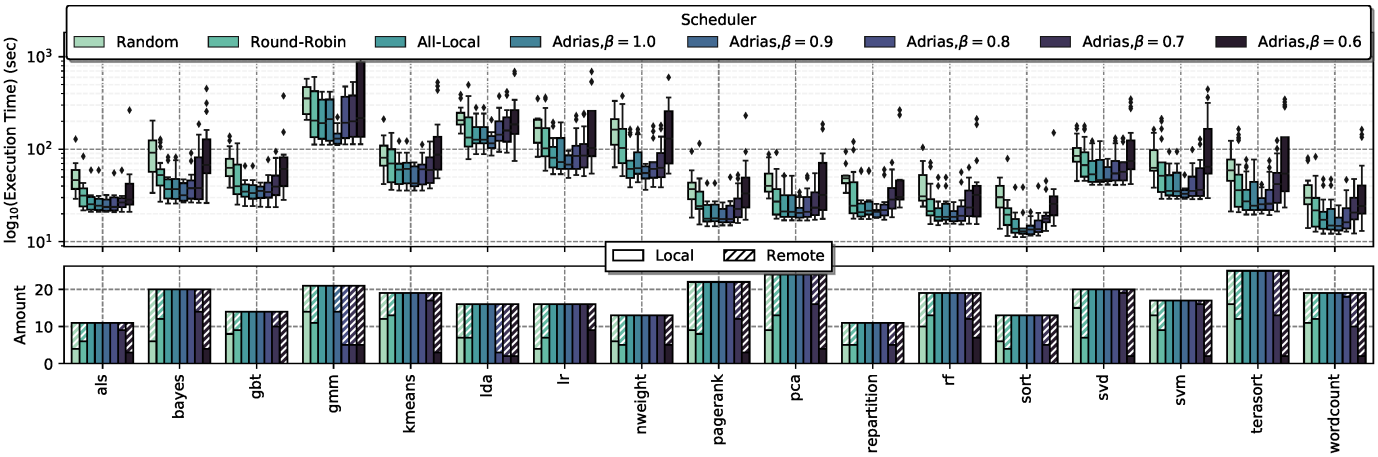
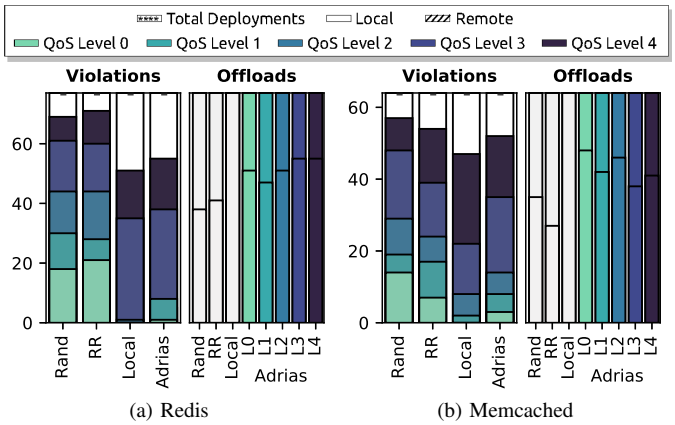


Fig. 16: Execution latency distribution of BE applications (top) and number of times that the application was deployed on local and remote memory (bottom) for different scheduling logics.



(a) Redis (b) Memcached

Fig. 17: Number of QoS Violations (left) and offloads (right) for Redis (a) and Memcached (b) benchmarks.

others by introducing almost no violations for looser QoS constraints and minimum number for stricter ones. For looser QoS levels (0-2), Adrias achieves similar results to the *All-Local* approach, by eliminating the majority of QoS violations, while offloading almost 1/3 of the applications to the remote memory. For stricter ones, Adrias provides comparable results with *All-Local* by introducing an average of 5% and 20% more QoS violations for Redis and Memcached respectively.

Adrias' impact on data traffic: Last, we quantify the amount of transmitted data over the FPGAs' network interconnection. Among all the examined scenarios, Adrias reduces the amount of transmitted data by 45% (β = 0.8) and 23% (β = 0.7) on average compared to Random and Round-Robin schedulers respectively. We note that in cases where Adrias offloads similar number of applications with the other schedulers, it generates up to 55% less traffic on the channel, revealing its tendency to favor less memory-intensive applications to be allocated on the disaggregated memory.

VII. Further Discussion Points

Why Deep Learning? Modern cloud data centers suffer from extensive and non-deterministic performance variability due to interference, workload diversity and HW heterogeneity [74], thus mechanistic or model predictive control approaches form highly expensive solutions due to the extensive simulations required to capture all the possible deployment scenarios [12]. To this end, ML-centric cloud platforms are attracting a lot of attention [9], [88], [95]. The rationale behind the employment of DL techniques is the automatic pattern discovery of neural networks; notably such patterns, able to discriminate performance indicators, could not be effectively set by typical human modeling or would require extensive scenario analysis. In particular, LSTMs have been proven to be extremely efficient on interpreting temporal patterns, i.e., interpreting system monitor time-series to actual performance metrics [30], [65].

Ability of Adrias to unveil human-driven remarks. During evaluation (Fig.16) we noticed that Adrias favors offloading certain applications to the remote memory (e.g., `gmm`, `lda`). While these applications present overlapping performance distributions between local and remote modes (Sec. V-B1), Adrias avoids offloading "non-overlapping" ones (e.g., `nweight`), which also suffer from stacked interference effects (R7). This verifies that Adrias properly models the inherent characteristics of the examined applications.

Adrias & HW heterogeneity. Adrias assumes no prior knowledge on the HW infrastructure, as any performance variability due to heterogeneity will directly affect the monitored metrics. For example, in case a system avails of both remote DRAM and NVMe, these would be considered by Adrias as two different memory tiers, with different latency characteristics. There is no requirement for Adrias to be aware of the actual medium backing each tier.

Adrias scalability. Due to the inherent HW limitations of the ThymesisFlow prototype, Adrias was evaluated on a single-node cluster. However, by design, Adrias is able to

scale on multiple nodes, where the monitoring (Watcher) and performance prediction (Predictor) components are distributed across the nodes of the cluster. The orchestration logic could be centralized (e.g., be integrated directly in the control plane of Kubernetes [13]), however, it should be adjusted in a straightforward manner to account for cluster-level efficiency in case of iso-QoS predictions between different nodes.

VIII. Conclusion

Hardware disaggregation is the next big step for efficient management of cloud infrastructures. In this work, we performed an extensive, interference-aware characterization for a set of cloud applications and highlighted the hidden pitfalls on a real memory disaggregated testbed. Driven by this analysis, we designed Adrias, a resource orchestrator for memory disaggregated cloud systems. Adrias leverages deep learning techniques to decide the memory mode of deployed applications. We showed that Adrias can efficiently utilize remote memory with minimal performance overheads.

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